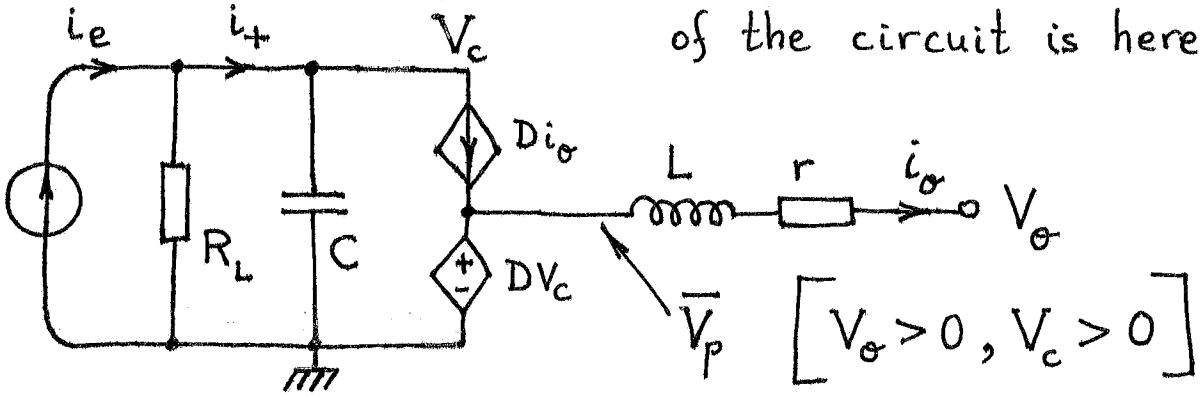
Control techniques in power electronics

WEEK 6

Controlling $V_c = V_+ - V_-$ (the higher voltage) in a DC/DC converter

We consider a canonical switching cell, with a nominal load R_L in parallel with the capacitor C, and $V_- = 0$ (hence $V_c = V_+$). The average model of the circuit is here:



Clearly, if $i_o > 0$ then power is flowing from left (high voltage) to right (lower voltage), and for $i_o < 0$ the direction of the power flow is reversed.
The current source may represent an energy source (such as an array of PV cells) if $i_e > 0$, or it may represent deviations of the load current from the nominal current flowing through R_L, if i_e is variable around 0. We want to control V_c.

$$\begin{cases} C\dot{V}_c = i_e - \frac{V_c}{R_L} - Di_o \\ L\dot{i}_o = -ri_o + DV_c - V_o \end{cases}$$

The terms Di_o and DV_c are non-linear (products).

As explained on p.13 of WEEK 3, we can linearize around an operating point, by considering small deviations dD, dV_θ, di_e from the operating point values D_0, $V_{\theta 0}$, i_{e0} :

$$D = D_0 + dD, \quad V_\theta = V_{\theta 0} + dV_\theta, \quad i_e = i_{e0} + di_e .$$

What we listed above are the input variables (V_θ and i_e are disturbances acting on the system, while D is the control input).

The state variables are V_c and i_θ. The operating point values V_{c0} and $i_{\theta 0}$ can be obtained from $D_0, V_{\theta 0}, i_{e0}$ by setting $\dot{V}_c = 0$, $\dot{i}_\theta = 0$:

$$\begin{cases} i_{e0} - V_{c0}/R_L - D_0 i_{\theta 0} = 0 , \\ -r i_{\theta 0} + D_0 V_{c0} - V_{\theta 0} = 0 . \end{cases}$$

Solving this system of equations (we omit the details) we obtain

$$\begin{cases} V_{c0} = \left(\frac{1}{R_L} + \frac{D_0^2}{r} \right)^{-1} \left(i_{e0} + \frac{D_0}{r} V_{\theta 0} \right), \\ i_{\theta 0} = \left(\frac{1}{R_L} + \frac{D_0^2}{r} \right)^{-1} \left(\frac{D_0}{r} i_{e0} - \frac{1}{R_L r} V_{\theta 0} \right). \end{cases}$$

We return to the differential equations on the bottom of p.1 and we write the corresponding linearized equations, also called small signal equations:

$$\begin{cases} C\, d\dot{V}_c = di_e - \frac{1}{R_L} dV_c - D_0\, di_\theta - i_{\theta 0}\, dD , \\ L\, d\dot{i}_\theta = -r\, di_\theta + D_0\, dV_c + V_{c0}\, dD - dV_\theta . \end{cases}$$

In the standard matrix form, we have

$$\frac{d}{dt}\begin{bmatrix} dV_c \\ di_\theta \end{bmatrix} = \underbrace{\begin{bmatrix} -\frac{1}{R_L C} & -\frac{D_0}{C} \\ \frac{D_0}{L} & -\frac{r}{L} \end{bmatrix}}_{A} \cdot \begin{bmatrix} dV_c \\ di_\theta \end{bmatrix} + \underbrace{\left[\begin{array}{cc|c} 0 & \frac{1}{C} & -\frac{i_{\theta 0}}{C} \\ -\frac{1}{L} & 0 & \frac{V_{c0}}{L} \end{array}\right]}_{B} \cdot \begin{bmatrix} dV_\theta \\ di_e \\ \hline dD \end{bmatrix}$$

(B_1 = first two columns, B_2 = last column)

The characteristic polynomial of A:

$$p(s) = \det(sI - A) = s^2 + a_1 s + a_0, \quad \text{where}$$

$$a_1 = -\operatorname{trace} A = \frac{1}{R_L C} + \frac{r}{L} > 0,$$

$$a_0 = \det A = \frac{1}{R_L C}\cdot\frac{r}{L} + \frac{D_0^2}{LC} > 0.$$

Notice that A is stable, since $a_1 > 0$ and $a_0 > 0$.

The relevant output is $V_c = [1 \;\; 0]\begin{bmatrix} V_c \\ i_\theta \end{bmatrix}$. The transfer function of the system is

$$\mathbf{P} = [1 \;\; 0](sI - A)^{-1} B, \qquad \mathbf{P} = [\mathbf{P}_1 \;\; \mathbf{P}_2],$$

where $\mathbf{P}_1 = [1 \;\; 0](sI - A)^{-1} B_1$, $\mathbf{P}_2 = [1 \;\; 0](sI - A)^{-1} B_2$.

Using that

$$(sI - A)^{-1} = \frac{1}{p(s)}\begin{bmatrix} s + \frac{r}{L} & -\frac{D_0}{C} \\ \frac{D_0}{L} & s + \frac{1}{R_L C} \end{bmatrix},$$

we obtain that

$$\mathbf{P}_2(s) = \frac{\widehat{dV_c}(s)}{\widehat{dD}(s)} = -\frac{i_{\theta 0}}{C}\cdot\frac{s + \frac{r}{L} + \frac{D_0 V_{c0}}{L\, i_{\theta 0}}}{p(s)}.$$

We see that P_2 has a <u>zero</u> at

$$z = -\frac{r}{L} - \frac{D_0 V_{c0}}{L\, i_{e0}} .$$

If $z < 0$ then the converter is easy to control (we shall return to explain this a little later). This is the case if $i_{e0} > 0$, i.e., the converter operates as a buck (power flows from left to right). If $z > 0$ (right half-plane zero) then, as we shall explain, it is much more difficult to find a good controller. This is the case only if $i_{e0} < 0$, i.e., the converter operates as boost.

We derive a <u>simpler expression for z</u> in the particular case <u>when $i_{e0} = 0$</u>. This means that we only have a resistor R_L on the left side at the operating point, so that $i_+ < 0$ and hence $i_{e0} < 0$. Now the formulas for V_{c0} and i_{e0} from p. 2 simplify to

$$V_{c0} = \left(\frac{1}{R_L} + \frac{D_0^2}{r}\right)^{-1} \cdot \frac{D_0}{r} V_{e0} ,$$

$$i_{e0} = -\left(\frac{1}{R_L} + \frac{D_0^2}{r}\right)^{-1} \cdot \frac{1}{R_L r} V_{e0} .$$

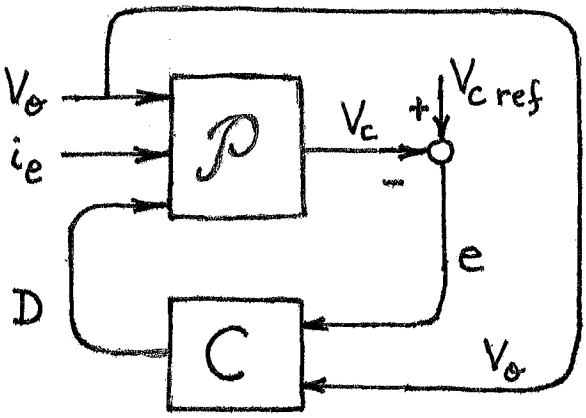
Substituting into the formula for z (on top of this page), we get

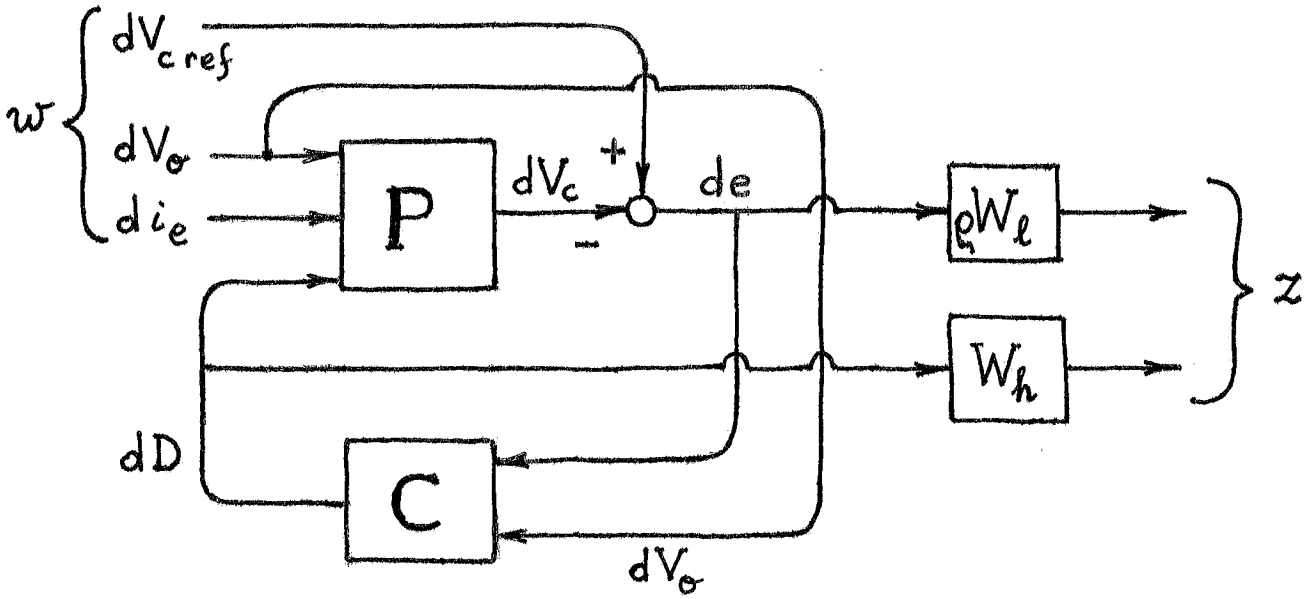
$$z = -\frac{r}{L} + \frac{D_0^2 R_L}{L} ,$$

which is usually > 0, since r is usually much smaller than R_L. This last formula for z is what usually appears in the literature.

Let V_{cref} be the reference signal for V_c, i.e.,

one aim of the controller is to make $e = V_{c\,ref} - V_c$ small. $V_{c\,ref}$ may be constant or slowly varying. The block diagram of the control system is shown here. In this diagram, we have denoted by $\mathcal{P}$ the nonlinear system (plant) described by the differential equations from p.1. For the design of the controller C, we use small signal model of the plant, represented by its transfer function $\mathbf{P} = [\mathbf{P}_1 \; \mathbf{P}_2]$, see p.3. Imposing a tracking requirement using the low-pass filter W_ℓ, and a robustness requirement using the high-pass filter W_h, see WEEK 2, we obtain the following standard H^∞ problem :

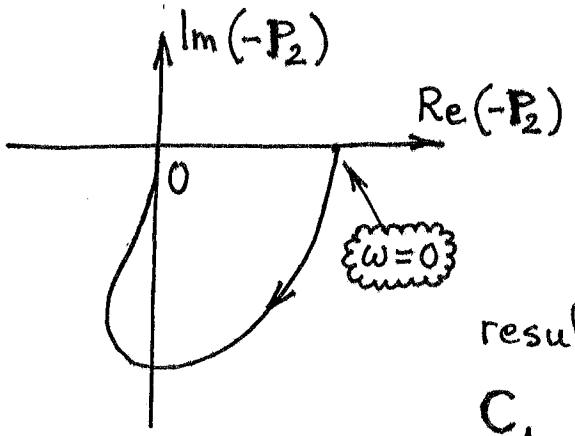




In principle, we could supply more information to the controller, such as i_e or i_o, but in my experience, this does not improve much.

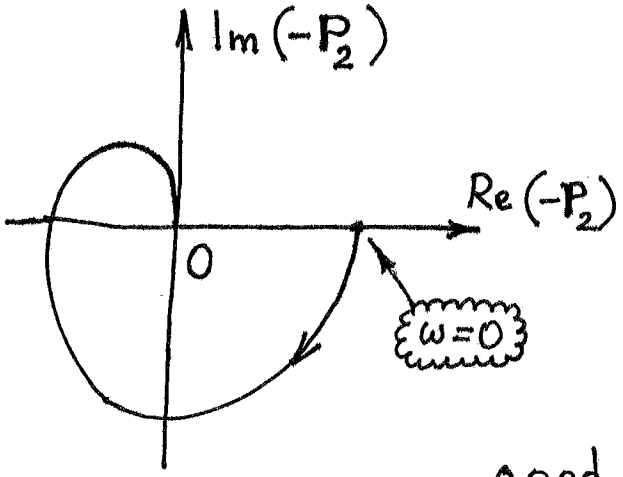
It is easy to see that the transfer function from $\begin{bmatrix} dV_\theta \\ di_e \end{bmatrix}$ to dV_c is $(1+P_2C_1)^{-1}(P_1 + P_2[C_2\ 0])$ (and from $\begin{bmatrix} dV_\theta \\ di_e \end{bmatrix}$ to de it is the same but with a $-$ sign).

If $z<0$, then the Nyquist plot of $-P_2$ looks like shown below, with $\arg(-P_2)$ going from $0°$ to $-90°$ but never going below $-180°$, hence $-P_2$ has infinite gain margin.



Thus, we can get good results even by choosing C_1 to be a large negative constant and $C_2 = 0$.

If $z>0$, then the Nyquist plot of $-P_2$ turns from $\arg(-P_2) = 0°$ to $\arg(-P_2) = -270°$, see below.



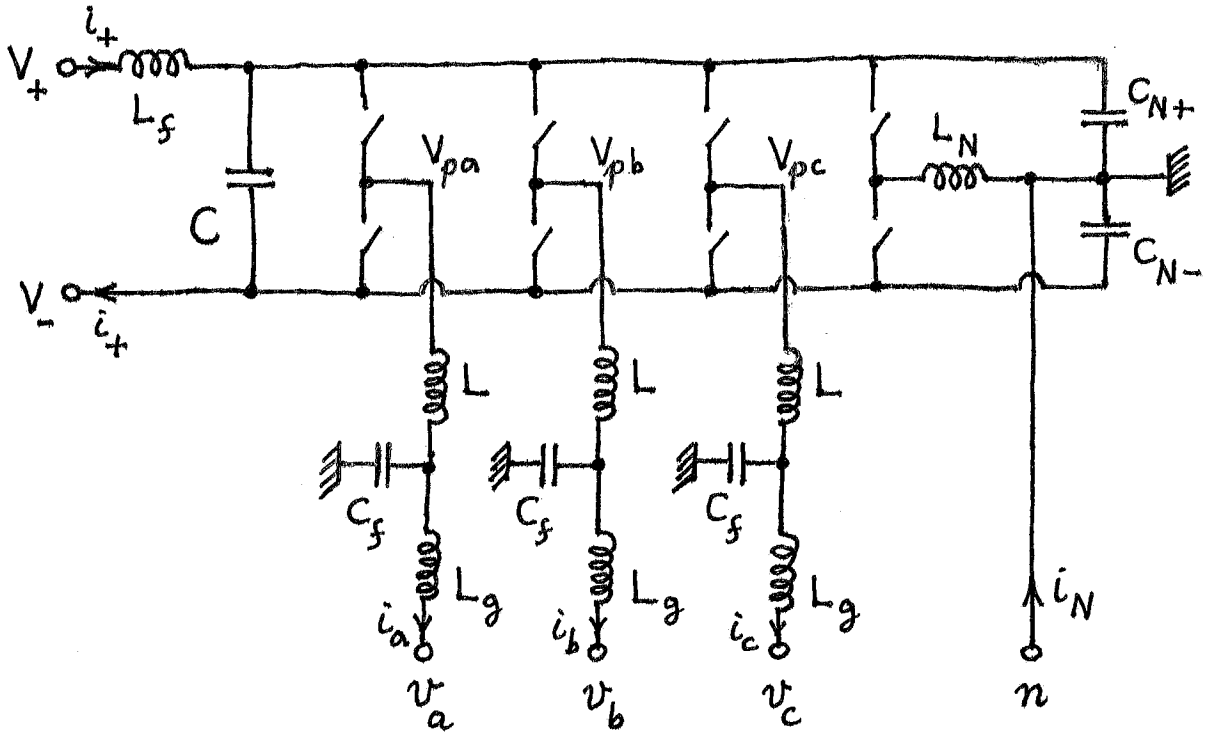
Now the gain margin is finite and may be small, which means that a constant controller cannot achieve satisfactory performance. Finding a good controller is now difficult, and it is in this situation that we really need H^∞ control theory.

Three-phase inverters – topologies and operation

"Inverter" means DC to AC converter (with the power possibly flowing either way). A three phase voltage (or current) means three voltages on three terminals that are (close to) being sinusoidal and with a phase shift of $2\pi/3$ between any two of them. The power distribution network (in all countries) is three-phase. One important advantage of a three-phase network over a single-phase network is that the power transmitted over a three-phase line is constant (or slowly varying), while for a single phase network the power oscillates at twice the network frequency (50Hz or 60Hz). Hence, the torque in a three-phase machine (generator or motor) is constant (or slowly varying). Three phase power distribution networks exist for more than 100 years.

A three-phase inverter may or may not provide a neutral line. Such a neutral line is needed if we want to allow a neutral current, which is the sum of the three phase currents, to flow back to the inverter. Balanced consumers, such as synchronous or induction motors, do not need a neutral line, as they have no neutral terminal.

We show below the circuit of a basic 3-phase inverter, with the optional circuit that provides a neutral line. Such a circuit (with neutral line) is also called a <u>three-phase four-wire inverter.</u>



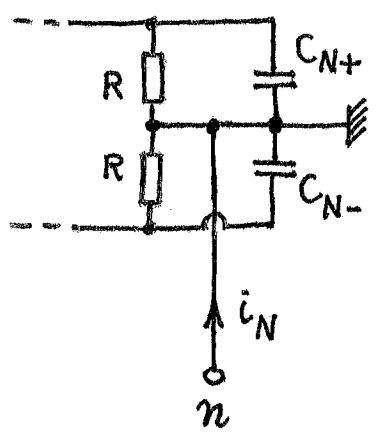
We see that each phase terminal is connected to the low voltage side of a canonical switching cell via the circuit formed by C_f and L_g. The capacitor C_f and the inductor L_g are optional (i.e., they may be absent). Their role is to reduce the ripple (see WEEK 3) both in the voltages v_a, v_b, v_c and in the currents i_a, i_b, i_c. Additionally, their presence makes the circuit easier to control, especially if we want to control the voltages on the capacitors C_f (because we have loads connected in parallel with these capacitors). The inductor L_f is also optional, and its role is to reduce the ripple current in i_+.

Note that the DC circuit connected to V_+ and V_- is assumed "floating", i.e., it has no additional connection to the AC circuit, except through the inverter.

The circuit on the right edge of our diagram is another canonical switching cell (with the inductor L_N) whose role is to keep the voltages on C_{N+} and C_{N-} equal. This way, the averaged voltages $\overline{V_{pa}}$, $\overline{V_{pb}}$ and $\overline{V_{pc}}$ can vary in a symmetric range around zero. This is only important if the neutral line is connected to the AC side. If the neutral line is connected and if the neutral current

$$i_N = i_a + i_b + i_c$$

has a DC component, then this may cause an imbalance between the voltages on C_{N+} and C_{N-} (i.e., V_+ will be different from $|V_-|$). If the neutral line is connected but we do not expect any DC component in i_N, then the circuit on the right edge of our diagram may be replaced with the following simpler (cheaper) circuit.



There will be some losses of power on the two resistors, but not much since R is large.

For the structure of each individual switch (MOSFET or IGBT with diode) we refer to p. 7 of WEEK 3.

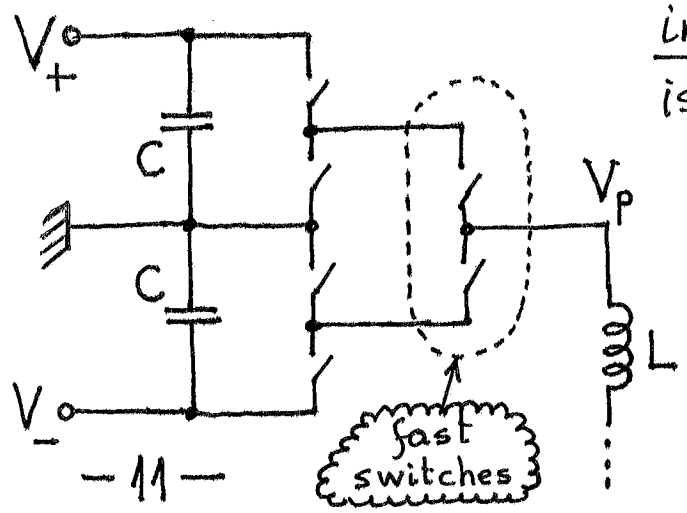
An inverter is called a <u>voltage mode inverter</u> if we are controlling the voltage on the AC side, and a <u>current mode inverter</u> if we are controlling the current on the AC side. For example, if the AC side is connected to the power distribution network, then we cannot control the voltage, only the current.

A few words about choosing the values L, C_f and the voltages. Let us denote the angular frequency of the AC voltage by ω_g, and the angular switching frequency by ω_s $(= 2\pi/\tau)$. The amplitude of $\overline{V}_{pa}$ is at most V_+ (but it should be less, to avoid the risk of saturation). At the frequency ω_g, the voltage on L_g is $\omega_g L_g i_a$ and on L it is approximately $\omega_g L i_a$ (we have neglected the capacitor current). These voltages should be small (less than 10%) of the phase voltage v_a, so that roughly, $\overline{V}_{pa} \approx v_a$. This imposes an upper bound on L_g, L. The current ripple through L can be estimated at $\tau V_+/2L$ (in the formula on top of p. 12, WEEK 3, we have taken $V_0 = 0$ and $D = 1/2$). The ripple current should be much less than i_a, and this imposes a lower bound on L. The resonant frequency $1/\sqrt{LC_f}$ should be much less than ω_s,

and also much more than ω_g, for obvious reasons. We have seen that the amplitude of v_a is $\approx$ the amplitude of $\overline{V_{pa}}$, which is less than V_+. Hence, the effective voltage of v_a must be less than $(1/\sqrt{2}) \cdot V_+$.

Each group of 2 switches in series in the circuit on p. 8 is called a <u>leg</u> (in particular, the two switches furthest to the right are called the neutral leg). Such a leg is usually sold as one unit, with protection circuits included (against too high current and too high voltage) and with the gate drivers included, with insulation between the logical signal q that comes from a processor (the PWM signal) and the high voltage circuit (to protect the processor).

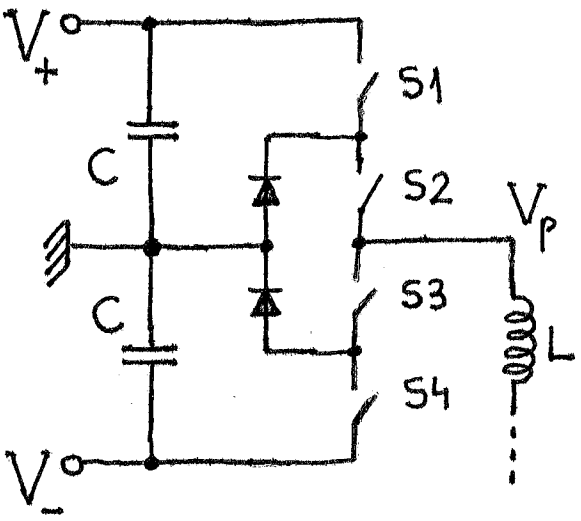
If we have several levels of DC voltage available, then it is advantageous to use them, by employing a <u>multi-level inverter</u>. Here we shall discuss some topologies for <u>three-level inverters</u>. The simplest is shown here, with only the circuit for one phase shown, containing 6 switches of which 2 operate fast, the others slowly.



The slow switches (which operate at the same frequency as the AC voltage) make sure that the fast leg is connected either between V_+ and 0 or between 0 and V_-. Only the fast switches will heat up (as most power is dissipated during the transitions).

Advantages: The ripple has been reduced to half. The maximal voltage that any switch sees is V_+ (as opposed to $2V_+$ in the circuit on p. 8). There is no need for a neutral leg and its associated circuit.

A clever alternative three-level inverter is the neutral point clamped inverter (also called a diode clamped inverter). Again we only show the circuit for one phase. Now we only need 4 switches per phase (as opposed to 6), all are fast.



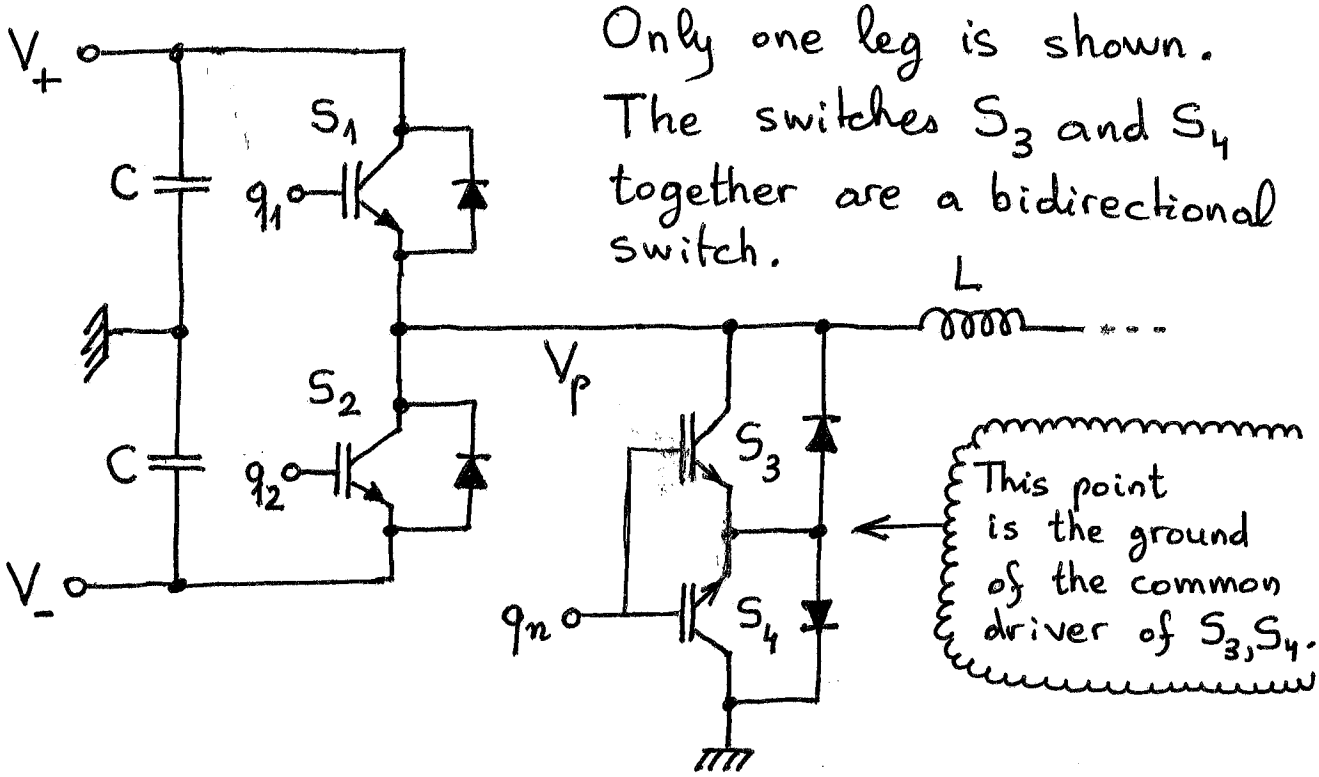
For $V_p = V_+$ we have to close S1 and S2.

For $V_p = 0$ we have to close S2 and S3.

For $V_p = V_-$ we have to close S3 and S4.

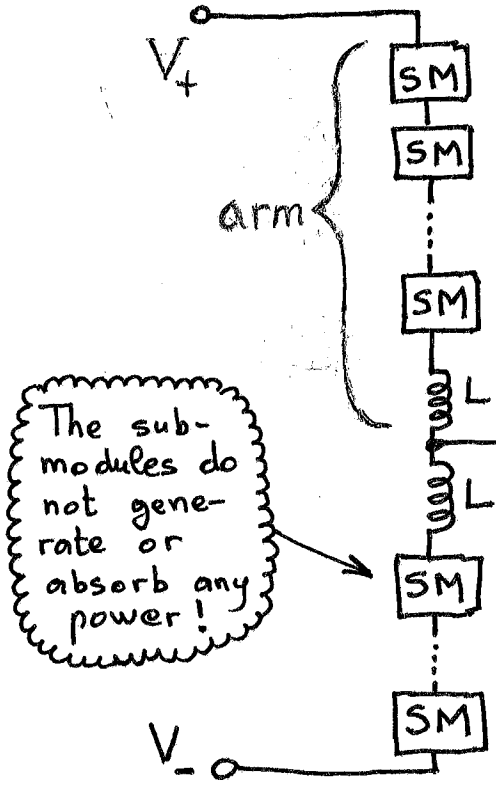
The advantages w.r.t. the two-level circuit on p. 8 are the same as for the previous circuit (listed on top of this page).

Here is an alternative way to build a neutral point clamped inverter.

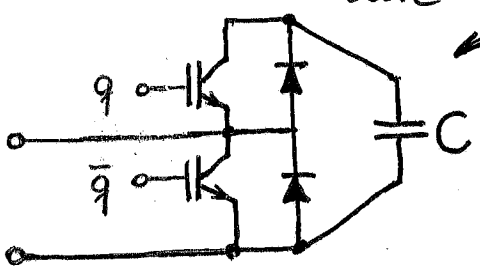


Only one leg is shown. The switches S_3 and S_4 together are a bidirectional switch.

A very promising new direction in high voltage DC inverters are the MODULAR MULTILEVEL CONVERTERS invented by Lesnicar and Marquardt in 2003.

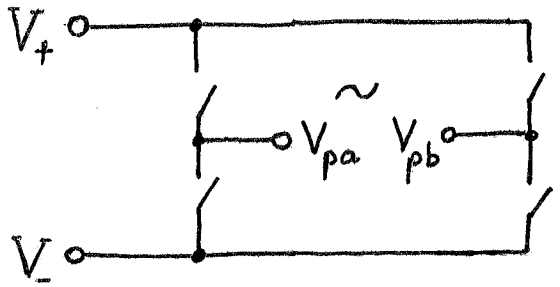


Only one leg is shown. Each submadule SM can switch between being a short circuit or an approximately constant voltage source, the simplest structure for SM



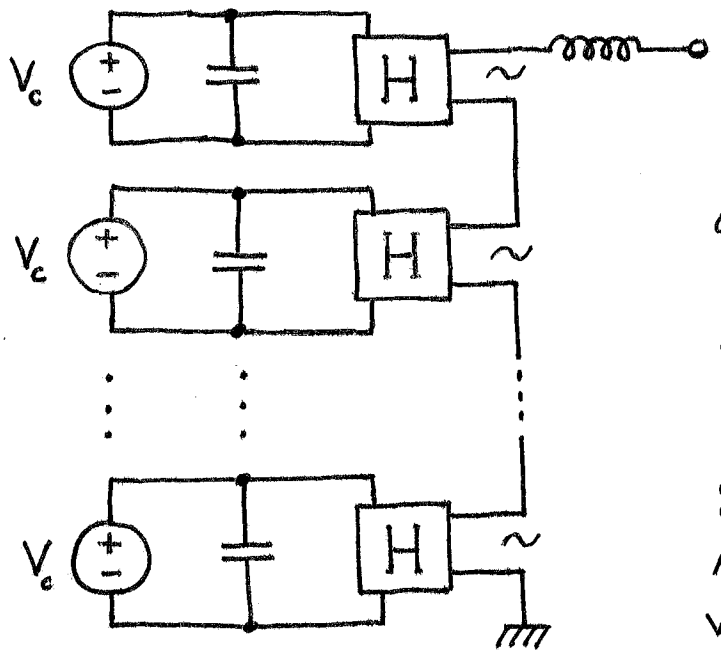
They are being switched slowly.

For single-phase inverters, the most common topology is the H bridge, consisting of 2 legs:

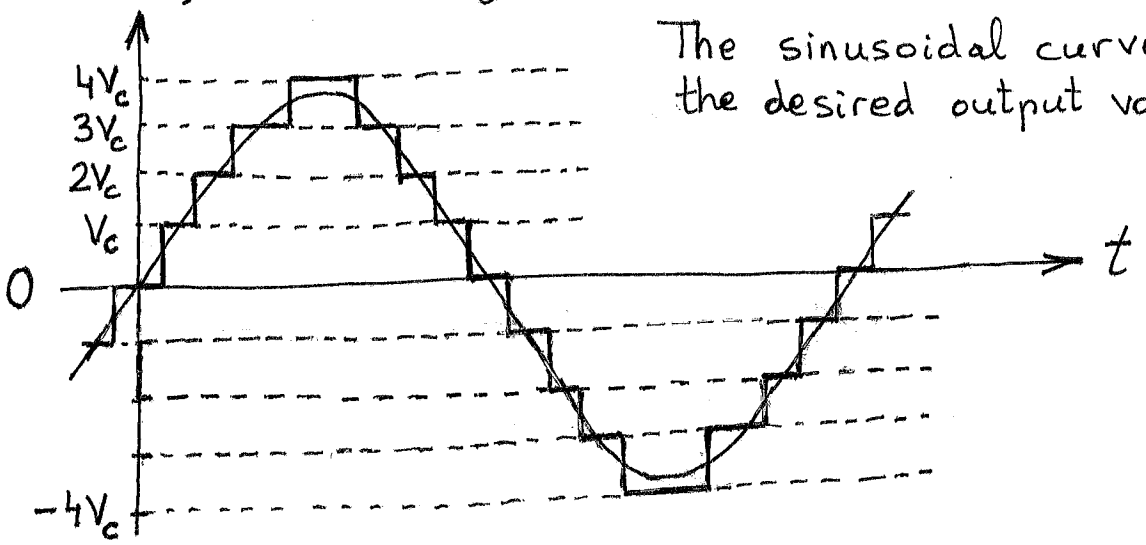


Denoting $V_c = V_+ - V_-$, we see that the voltage between V_{pa} and V_{pb} may be V_c, 0 or $-V_c$. Thus, we can generate an AC signal $\overline{V_{pa}} - \overline{V_{pb}}$ (the averaged signal) that has an amplitude of up to V_c (as opposed to $V_c/2$ for each leg of the circuit on p. 8). Of course, to get an inverter, we also have to connect a capacitor C between V_+ and V_-, and an inductor L in series with either the terminal V_{pa} or with V_{pb}.

We can build an inverter using several independent DC voltage sources and H bridges, as shown below (such an inverter usually transfers power from DC to AC, or it generates only reactive power). We have only drawn one phase of a possibly three-phase inverter. There are many different possibilities for sharing the voltage (and hence the power) between the H bridges. One is to share equally. Another possibility is to divide the total (sinusoidal) average voltage into many shallow rectangles, and each H bridge generates one such rectangle in each half-wave, hence slow switching.

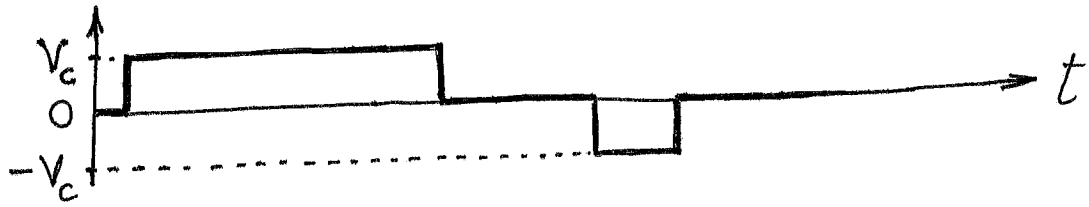


We show this here, assuming that we only have four H bridges in series:

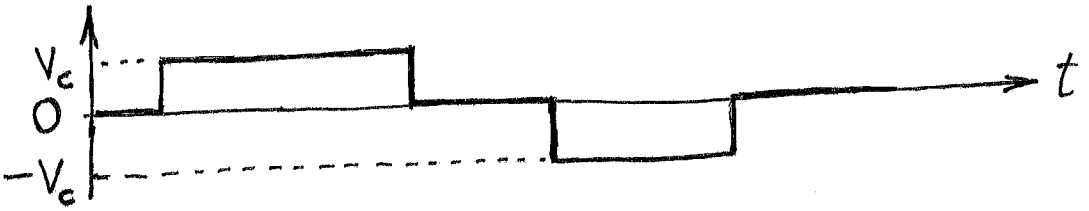


The sinusoidal curve is the desired output voltage.

The output voltage of the first H bridge:



The output voltage of the second H bridge:



Clearly, for more H bridges, the approximation of the sine wave gets better.